2021 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) | 978-1-6654-1934-5/20/$31.00 ©2021 IEEE | DOI: 10.1109/VLSI-TSA51926.2021.9440127

DFT Models of Ferroelectric Hafnium-Zirconium Oxide Stacks With and Without Dielectric Interlayers

Kisung Chae[1,2], Andrew Kummel[1], Kyeongjae Cho[2]

[1] Department of Chemistry and Biochemistry, University of California San Diego, 9500 Gilman Dr, La Jolla, CA 92093
[2] Department of Materials Science and Engineering, The University of Texas at Dallas, 800 W Campbell Rd, Richardson, TX 75080
E-mail: kichae@ucsd.edu

INTRODUCTION

Endurance is a key material performance metric for device and memory applications and is diminished due to defect formation. Defects alter material properties and relative phase stability, adversely affecting the reliability of devices. Ferroelectric field-effect transistors (FEFETs) have metal-insulator-semiconductor (MIS where I=ferroelectric) gate stacks which typically show unsatisfactory endurance of about 10^5 cycles,[1] while metal-insulator-metal (MIM where I=ferroelectric) capacitors can demonstrate endurance up to 10^{12}. Adding a linear dielectric (DE) interlayer at the FE-semiconductor interface may enhance the endurance by suppressing defect formation due to oxygen vacancies,[1] but the electrostatic role of the DE interlayer has not been clearly examined yet. Here, DFT is employed to develop an atomic and electronic level understanding of the behavior of atoms in MIM and MIS stack models with and without DE interlayers due to polarization switching.

ATOMIC STACK MODELS

To construct hafnium-zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$; HZO) MIM and MIS stack models, nickel (Ni) and silicon (Si) were chosen to serve as metal and semiconductor electrodes. MIM and MIS devices were modeled as Ni-HZO-Ni and Ni-HZO-Si, respectively. The orthorhombic $Pca2_1$ phase of HZO is the FE layer, and the cubic $Fm\bar{3}m$ phase of HZO was chosen as the linear DE interlayer for its atomic structural compatibility with the FE layer at FE/DE interfaces. Stack models were made with the polarization direction in the FE layer along with the stacking direction, i.e., HZO (001), and atoms in the middle were fixed to keep the spontaneous dipoles from rotating to the side due to the unfavorable electrostatic interactions between the FE and DE layers. Note that HZO is typically grown along (111), and there is always a polarization component along the growth direction. The HZO (001) model is used here for the clarity of model analysis. Ni (001) and Si (001) were also used for the stacks. The lattice spacings of each layer along lateral directions were fixed at the lattice parameters of the FE HZO; therefore, the unit cells of Ni and Si were strained along the lateral directions, while the vertical direction and internal atomic coordinates were relaxed.

MIM AND MIS STACK MODELS

Figure 1 shows the MIM and MIS stack models with two possible polarization states, i.e., up and down, in which FE HZO is in direct contact with metal and semiconductor. Note that the O atoms in the FE HZO are displaced relative to the Hf/Zr atoms when the polarization switches, and the displacements of the interfacial O atoms or bridging O atoms may cause charge transfer, bond strains and even bond breaking. Consecutive polarization switching *via* external bias voltage, which is a typical device operation condition, would promote defect generation by repeated bonding changes at the FE HZO interfaces. Such defects would introduce defect-induced gap states, and their diffusion into HZO alter the relative stability of the FE HZO, degrading device performance.

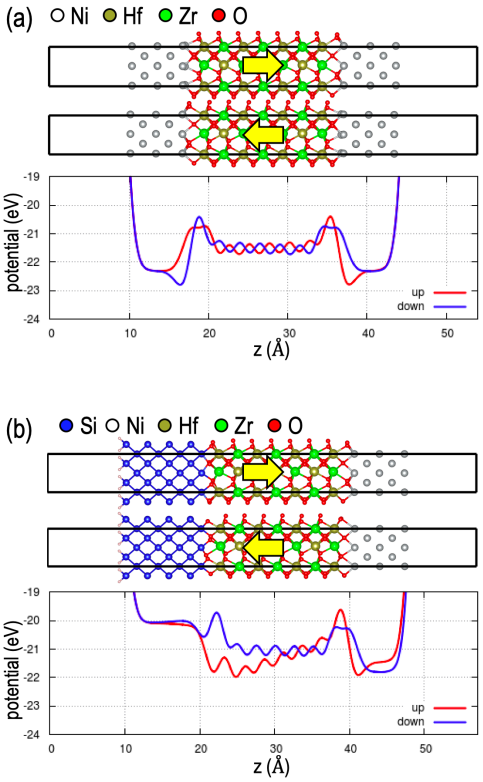

Fig. 1. MIM and MIS stack models with FE in direct contact with metal and semiconductor. Yellow arrows on HZO indicate polarization orientations: (right) up and (left) down. Potential profiles acting on electrons are shown below the atomic models. Negligible potential gradients in both polarization states for MIM stacks indicate excess charges at the interfaces are accommodated by the metals, while a finite field buildup is shown for MIS stacks with polarization up due to the small density of states at the Fermi energy and directional bonding of Si.

The different endurance behaviors seen in MIM and MIS can be attributed to different electronic structures and the different bonding character between metal and semiconductor at HZO interfaces. First, metals show a finite density of states at Fermi energy and are capable of accommodating fluctuations in the carrier density. Conversely, negligible electronic states are found at the Femi level for semiconductors; therefore, a significant internal field readily accumulates in the FE even with a small amount of excess charge. Second, Si bonds are more directional because they are covalent compared to the non-directional metallic bonds in Ni; therefore, smaller bond strains would be induced for MIM than MIS, and bond strain can be a source of defect generation.

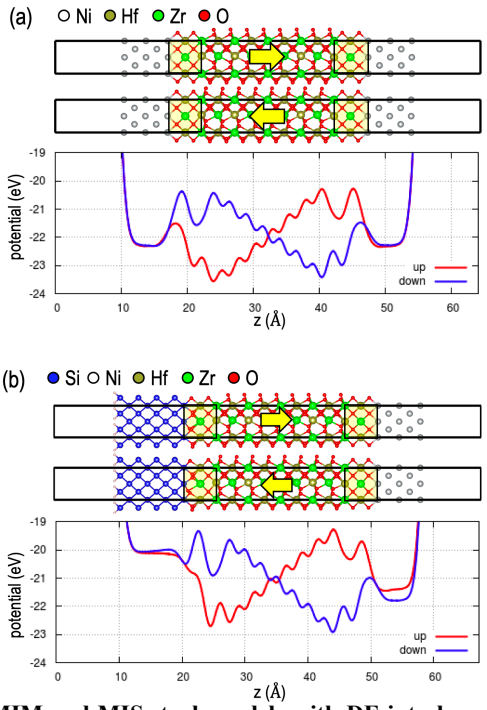

Fig. 2. MIM and MIS stack models with DE interlayers at the interfaces. DE interlayers (cubic phase of HZO) are indicated by yellow boxes. Significant potential gradients in the FE layers are induced by the DE interlayers, and would be a source of defect generation and device failure.

The DFT potential profiles for MIM and MIS stacks (Fig 1) are consistent with low field in MIM and high field in MIS structures. MIM stacks show flat potential profiles inside the FE layer, indicating that excess charges at the interfaces due to spontaneous dipoles in the FE are accommodated by the direct metal contact. Conversely, a finite potential gradient is observed for MIS stacks with polarization up, indicating the internal field buildup is due to the uncompensated charges. Unlike MIM, MIS shows asymmetric potential profiles with respect to polarization state, which is partly due to the presence of interface dipoles at the HZO/Si interface.[2] Polarization switching induced an interfacial Si bonding change from covalent to partly ionic with a nominal valence charge state of +2 forming an interface dipole. The interface dipole is either added or subtracted to the FE polarization resulting in an asymmetric potential profile with respect to polarization switching.

Effects of DE Interlayers

A significant internal field is induced inside the FE layer when the linear DE interlayer is added at the FE interfaces of both MIM and MIS stack models as shown in Fig. 2. The field strengths in both cases are computed by a linear fitting of the potential profile as about 18 MV/cm, which exceeds the breakdown voltage of 13 MV/cm for bulk HfO_2.[3] The charge-compensating effects of the metal layers as described above vanish when the FE and metal are separated by the DE interlayer with a sub-nanometer thickness. The large induced field will have adverse effects on device operation such as charged defect generation to compensate the internal field and DE breakdown due to Zener or avalanche effects. Therefore, it is critical to prevent an uncontrolled DE formation at the interface for enhanced device performance.

For FE HZO MIM capacitors, TiN is generally used as a metal electrode for which a relatively abrupt interface can sometimes be grown without forming a thin DE interlayer; however, other metal electrodes may be even better. Conversely, interfacial SiO_2 would be readily formed at the Si/HZO interface at an elevated temperature, e.g., during typical post-deposition annealing at 400-600°C.[2] Once formed, the SiO_2 interlayer will induce a large field in the FE layer, resulting in defect formation, ferroelectricity loss, and device failure.

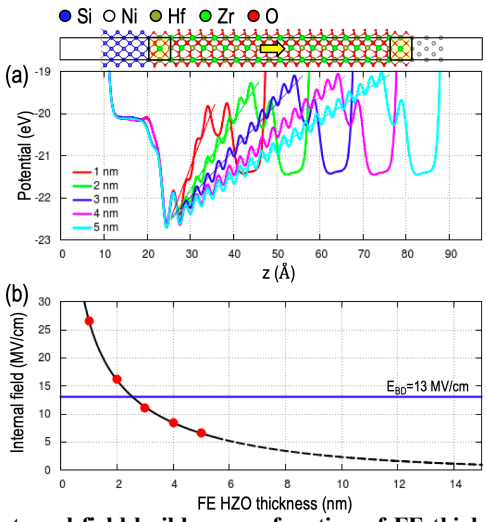

Fig. 3. Internal field buildup as a function of FE thickness. (a) The potential gradient inside the FE decreases with an increasing FE thickness. (b) Strength of the internal field is computed by a linear fitting within the FE region, and is clearly shown to decrease with an increasing FE thickness. The blue line indicates the breakdown voltage of bulk HfO_2 of 13 MV/cm.[3] The internal field is extrapolated to thicker FE layers as shown in dashed line.

FE Thickness Scaling

The MIS stack models were employed to study thickness effects of the FE layer. A decreasing internal field strength with increasing FE thickness is clearly demonstrated as shown in Fig. 3. The field strength is exceedingly high for 1-3 nm FE layers but is greatly reduced for the thicker (>5nm) FE layers. This analysis is consistent with the reported FE HZO high cycle devices being 4 nm or thicker, while reported sub 4 nm HZO films are characterized by low cycle piezoresponse force microscopy.[4] As shown in Fig. 3, the internal field in the 1-3 nm FE layer would generate defects upon cycling and lower the endurance behavior. Thicker HZO films would have lower internal field strength, but stabilization of FE phase with respect to other phases might be difficult as the stabilization of the FE phase would stem from the interface effects and higher voltage operation is also required.[5] Therefore, optimizations of the thickness scaling as well as device fabrication processing conditions for the HZO films must be further investigated to maximize both ferroelectricity and stability of the devices.

This work has been supported by SRC JUMP ASCENT (Task No. 2776.059).

References

[1] W. Xiao *et al.*, *Nanoscale Res Lett*, **14,** 25, (2019)
[2] N. Miyata, *Materials*, **5**, 512–527 (2012)
[3] C.-H. Chang and J.-G. Hwu, *IEEE Trans. Device Mater. Relib.*, **9**, 215–221 (2009)
[4] S. S. Cheema *et al.*, *Nature*, **580,** 478–482 (2020)
[5] K. Chae *et al.*, *J. Appl. Phys.*, **128,** 054101 (2020)